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Short communication

# Silicon carbide nanowires as highly robust electrodes for micro-supercapacitors

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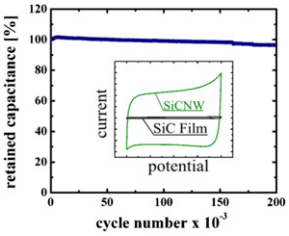
## HIGHLIGHTS

- Demonstration of silicon carbide as aqueous supercapacitor electrode.
- Performance results are presented.
- Silicon carbide electrode proven as a robust aqueous supercapacitor electrode.

## GRAPHICAL ABSTRACT

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## ABSTRACT

The effectiveness of silicon carbide (SiC) nanowires (NW) as electrode material for micro-supercapacitors has been investigated. SiC NWs are grown on a SiC thin film coated with a thin Ni catalyst layer via a chemical vapor deposition route at 950 °C. A specific capacitance in the range of ~240 μF cm$^{-2}$ is demonstrated, which is comparable to the values recently reported for planar micro-supercapacitor electrodes. Charge–discharge studies demonstrate the SiC nanowires exhibit exceptional stability, with 95% capacitance retention after 2 × 10$^5$ charge/discharge cycles in an environmentally benign, aqueous electrolyte.



## 1. Introduction

With the development of autonomous micro-sensors and actuators and distributed sensor networks, there has arisen a need for compact microscale, integrated, and reliable power sources. Micro-batteries are under development for these applications; however, they are still susceptible to typical battery failure modes leading to lifetimes of ~10$^3$ cycles [1]. This aspect is especially unattractive for remote sensors in locations which are difficult to service such as those embedded in civil structures, oil wells or living bodies. Batteries also suffer from the potential for over-heating during operation under high charge/discharge rates, [2] which is problematic for uses which require frequent high-power energy bursts for data relay. In this context, supercapacitors (also known as ultracapacitors) offer several advantages. Since their

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storage mechanism, based on electrochemical double layer capacitance, is purely electrostatic, they possess long cycle life times on the order of $10^6$ (vs. $10^3$ for Li-ion batteries). In addition, high specific power ratings (~10× that of Li-ion batteries) [3] are achievable without the associated heat of a chemical reaction which makes supercapacitors preferable for use in combination with devices drawing frequent high power loads.

Several planar micro-supercapacitors have already been reported in the literature [4–12]. A major challenge of developing such planar devices is the device-level integration of the electrode material. Activated carbon, which is the most common material used in macroscale supercapacitors, is difficult to integrate in planar technology, due to such issues as precise placement and the uniformity needed to pattern the electrode [5]. As a consequence, for on-chip supercapacitor development, research has focused on nanomaterials such as carbon nanotubes [4], graphene [8], or nanowires (NWs) [7], which are by nature high surface area materials and compatible with standard microfabrication techniques. However, carbon-based nanomaterials are hydrophobic, and hence present electrode wetting issues, and silicon NW electrodes corrode readily in aqueous electrolytes [7]. These are major shortcomings, given that aqueous electrolytes provide higher power capabilities than non-aqueous alternatives (e.g., organic or ionic liquid based electrolytes), are environmentally benign and may be biocompatible. Due to the corrosion issue, Si NW supercapacitors have only been demonstrated in non-aqueous electrolytes [12]. Microfabricated carbon post interdigitated electrodes generated from photoresist pyrolysis have also received attention [10,11]. These materials are much larger in scale with heights of ~100 μm and diameters of ~50 μm. After electrochemical activation they are hydrophilic and demonstrate higher specific capacitance than the nanomaterials discussed above. However this is due in part to pseudocapacitive contributions and at best they show capacitance fade of over 10% after only 1000 charge/discharge cycles.

This paper reports the performance of silicon carbide nanowires as electrode materials in aqueous electrolyte for micro-supercapacitors. SiC is known to be a wide-bandgap semiconductor material with excellent physicochemical stability, and is compatible with standard microfabrication techniques [13]. The results in this paper show that the SiC NWs exhibit specific capacitance values in aqueous electrolytes that are comparable to the recently published carbon nanomaterial-based micro-supercapacitors mentioned above [4,7,8]. The SiC nanomaterials here are less than 10 μm thick and can withstand $2 \times 10^5$ charge/discharge cycles in aqueous electrolyte while maintaining over 95% of their initial capacitance value. Together these properties make SiC NWs a promising candidate for aqueous micro-supercapacitor applications which require extremely robust performance and thin form factors.

## 2. Experimental

Silicon carbide nanowires presented in this paper are grown on n-doped 3C-SiC thin (2 μm) films on a Si(100) substrate with a $SiO_2$ (1.5 μm) isolation layer. The 3C-SiC thin films are deposited in a low-pressure chemical vapor deposition (LPCVD) reactor, employing methylsilane as the precursor and in-situ doped using ammonia [14]. The SiC NWs are grown by a Ni-catalyzed CVD process similar to that reported in Ref. [15]. More specifically, a thin layer of nickel (~2.2 nm) is deposited by e-beam evaporation on the $SiC/SiO_2/Si(100)$ substrates. This layer acts as the catalyst for the SiC NW growth [15]. Samples are placed inside an LPCVD reactor and temperature is increased to 950 °C at a rate of about 55 °C $min^{-1}$ under 10 sccm of $H_2$. When the growth temperature is reached, methyltrichlorosilane (MTS) is introduced in the tube at a flow rate of 0.5 sccm while the $H_2$ flow rate is reduced to 5 sccm. The growth step proceeds for 30 min. At the end of the growth, the $H_2$ flow rate is increased to 10 sccm while MTS flow is stopped. Samples are then cooled down to room temperature at a rate of about 15 °C $min^{-1}$. The pressure is maintained at approximately 5 Torr throughout the growth process.

Nanowire morphology is characterized by scanning electron microscopy (SEM) using a LEO 1550. Crystal structure is determined using a Siemens D5000 automated X-ray diffractometer (XRD) operated in $\theta-2\theta$ geometry. For the XRD analysis, the nanowires are grown directly on a Si(111) substrate to avoid interference with signal obtained from the underlying SiC thin film. High resolution transmission electron microscopy (HRTEM) is performed using the FEI Tecnai monochromated transmission electron microscope (TEM) operating at 200 kV.

Capacitive performance of the nanowires is evaluated using an electrochemical workstation (CH Instruments Inc., 660D) in a 3-electrode configuration. Electrical connection to the nanowire samples is made through the n-doped SiC thin film ($\rho = 0.01\ \Omega$ cm) on which the nanowires are grown. During catalyst evaporation, a part of the sample is masked in order to create a nanowire-free area which is used for this connection. A platinum wire is used as the counter electrode and an Ag/AgCl electrode is used as the reference electrode. All measurements are performed in an aqueous electrolyte solution of 3.5 M KCl. Prior to acquisition, samples are cycled ten times to ensure removal of any adsorbed contaminants.

## 3. Results and discussion

Fig. 1a shows a representative SEM image of the nanowire arrays grown. A dense film of NWs is achieved with an average thickness of ~6 μm and the wires appear somewhat tapered. An XRD

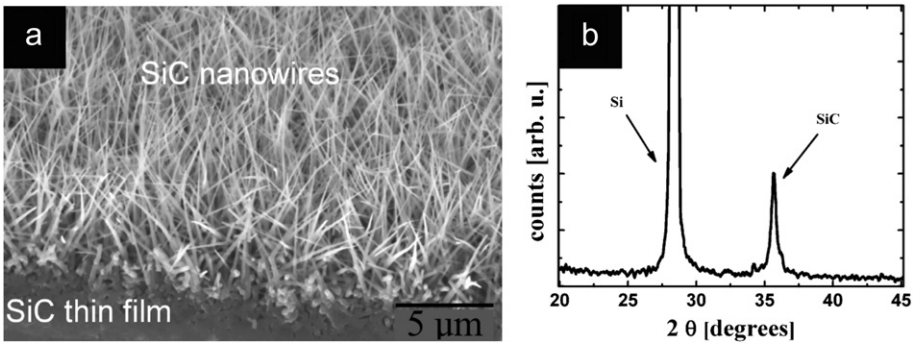


**Fig. 1.** a) SEM image of the SiC nanowires grown on a SiC thin film. b) XRD spectrum of SiC nanowires grown on a Si(111) substrate.

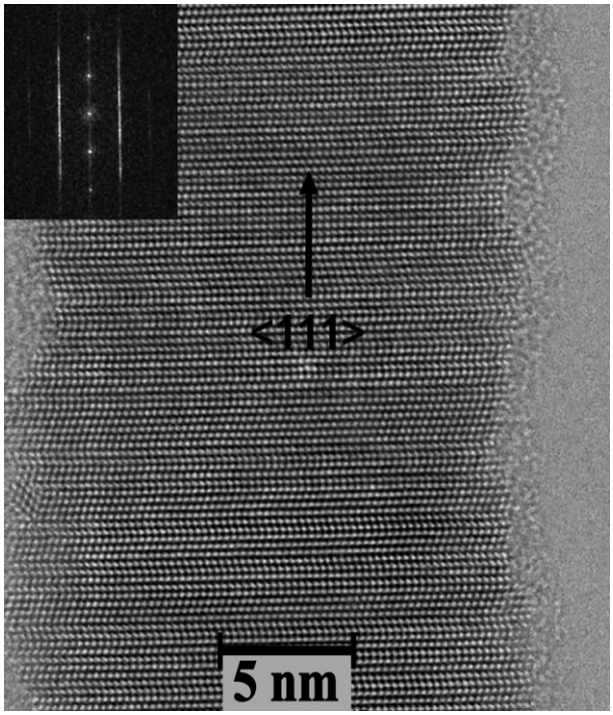


**Fig. 2.** HRTEM characterization of a SiC nanowire. Inset shows the corresponding Fourier transform.

spectrum of nanowires grown on a Si(111) substrate is shown in Fig. 1b. Two peaks are noticeable in the range 20-90°, namely the Si(111) peak at 28.5° and the SiC peak at 35.7°. A strong peak near 35.7° corresponds to the lattice spacing between SiC bilayer stacks along the <111> growth direction of β-SiC or <0001> direction of α-SiC, and does not allow one to distinguish between cubic and hexagonal phases [17,18]. The full width-at-half-maximum values for Si and SiC peaks, at 28.5° and 35.7° respectively, after subtracting the $K\alpha_2$ peak, are 0.1° and 0.43°, with 0.1° being the minimum resolution of the XRD system. This is indicative of the good crystalline quality of the SiC nanowires. The XRD results are confirmed by high resolution TEM characterizations performed on single NWs dispersed in ethanol by sonication (see Fig. 2). These micrographs show that the SiC nanowires grow along the <111>–3C axis with a high density of stacking faults associated with the presence of 2H SiC polytypes. Lines on each side of the <111>–3C axis in the Fourier transform of the image confirm the presence of stacking faults (see Fig. 2 inset).

Supercapacitors store energy at the interface between the electrodes and the electrolyte, in what is called the electric double layer (EDL) [3]. The capacitance of such devices is then directly proportional to the surface area of the electrodes' material. Thus, by using high surface area materials such as nanowires, high capacitance values are expected. Cyclic voltammetry (CV), in the voltage range of −0.2 to 0.6 V vs. Ag/AgCl reference, is employed to determine the contribution of the nanowires to the total measured capacitance of the sample (see Fig. 3a). Capacitance per projected area is calculated by:

$$C = \frac{i}{\mathrm{d}V/\mathrm{d}t}\cdot\frac{1}{A} \tag{1}$$

where $i$ is the current at $V = 0.2$ V during the positive sweep, $\mathrm{d}V/\mathrm{d}t$ is the scan rate used for the measurement, and $A$ is the projected surface area of the sample immersed in the solution. Choosing to read the current at 0.2 V leaves out any pseudocapacitive contribution from redox reactions which may be occurring at the extremes of the voltage range and is thus a good estimate of the pure double layer capacitance of the sample. Fig. 3a shows a comparison of CV results between the SiC NW-on-SiC/$SiO_2$/Si and the SiC/$SiO_2$/Si samples. The measured capacitance of the NW sample at 100 mV $s^{-1}$ is ∼38 times higher than the SiC thin film alone. This corresponds to SiC NWs exhibiting a specific capacitance value of ∼240 μF $cm^{-2}$ projected area, comparable to the results obtained on carbon nanotube arrays (∼430 μF $cm^{-2}$ for ∼80 μm thick film) [4] or carbide-derived carbon films (∼740 μF $cm^{-2}$ for ∼1 μm thick) [6]. Furthermore, the lack of any significant oxidation peaks in the cyclic voltammetry results [16] indicates that there is no electro-chemically active nickel remaining on the SiCNW samples.

In order to evaluate the charge/discharge behavior of the SiC NW arrays, galvanostatic discharge studies have been performed. A constant charge and discharge current is utilized to cycle the electrodes between −0.2 and 0.6 V. Fig. 3b reports the charge/discharge data obtained. The initial vertical voltage drop region during discharge cycling may be attributed to the electrode series resistances. With increasing current this voltage drop increases as expected. By analyzing the slope of the discharge curve, the capacitance may be calculated from equation (1). The specific energy stored in the electrode is determined from the calculated capacitance by:

$$E = 1/2CV^2 \tag{2}$$

where $E$ is the energy per specific area and $V$ is the total voltage window discharged over. Specific power may then be determined by:

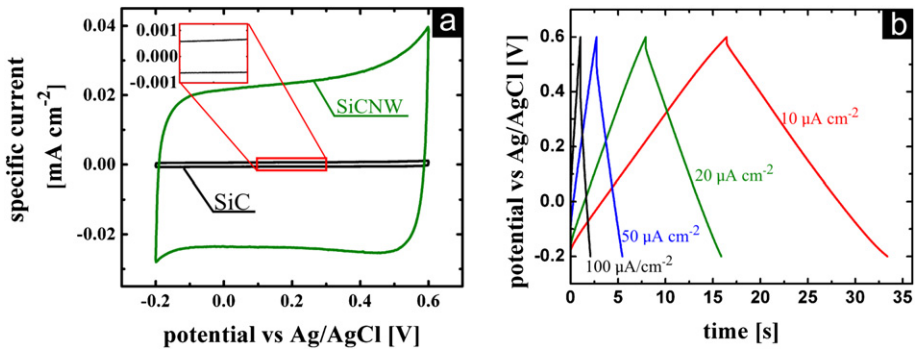


**Fig. 3.** a) CV results for SiCNW and planar SiC electrodes. Scan rate was 100 mV $s^{-1}$. The inset is a close up view of the SiC film results. The *y*-axis uses a scaled axis with the same units as the main graph. The *x*-axis has not been changed and is centered at 2.0 V. b) Galvanostatic discharge results for SiCNW electrode over a range of discharge/charge currents.

$$P = E/t \quad (3)$$

where $P$ is the power per specific area and $t$ is the total time for discharge. The useable stored energy drops off as the current is increased due to an increasing voltage drop from the series resistances in the system. Hence it is important to report the specific power achieved at a specific energy stored. From the galvanostatic discharge results, the electrodes tested here exhibit a specific energy of ~68 μJ cm$^{-2}$ and specific power of ~4 μW cm$^{-2}$ at the discharge current of 10 μA cm$^{-2}$, the lowest current tested. At the highest current tested, 100 μA cm$^{-2}$, the electrodes yield a specific energy of ~41 μJ cm$^{-2}$ and specific power of ~40 μW cm$^{-2}$. The power value is limited by the resistance of the electrode in this configuration which is found to be ~1300 Ω for a ~0.8 cm$^2$ sample, as determined from the voltage drop in the galvanostatic discharge [19] at 10 μA cm$^{-2}$. This limitation also affects the capacitance as discharge rate is increased which can be observed from the results of cyclic voltammetry performed over a wider range of scan rates presented in Fig. 4. As the scan rate exceeds 200 mV s$^{-1}$, the resulting current–potential graph becomes less rectangular and more skewed, implying uncompensated internal resistances. The capacitance drops from ~240 μF cm$^{-2}$ at 100 mV s$^{-1}$ to ~135 μF cm$^{-2}$ at 1 V s$^{-1}$. Efforts are ongoing to reduce this resistance by in-situ doping of the nanowires or graphitization of the SiC thin film prior to nanowire growth [20].

In order to evaluate the cycle life of the nanowires, 2 × 10$^5$ charge/discharge cycles have been performed on a sample using cyclic voltammetry at a scan rate of 5 V s$^{-1}$. The samples are cycled over the whole charge/discharge voltage window of −0.2 to 0.6 V. This is important to note as degradation via redox reactions may not occur in a voltage window limited to be smaller than the operational voltage window. Fig. 5 reports the percent retained capacitance as a function of the cycle number. This test reveals an extremely stable behavior, with a capacitance loss smaller than 5% after 2 × 10$^5$ charge discharge cycles. This is superior to carbon based electrodes, such as in Ref. [10], which show >12% capacitance loss after one thousand cycles. In this regard, SiC nanowires are also superior to silicon NW arrays that are found to corrode readily during cyclic voltammetry under the same conditions [7]. The one step processing of these materials is also favorable compared to the two step silicon NW formation followed by SiC coating in order to mitigate aqueous corrosion reported elsewhere [7]. The capacitance values of the SiC nanowires presented here are comparable to the SiC coated silicon NWs of similar length (~440 μF cm$^{-1}$ for ~7 μm long wires) [7]. The long cycle life reported in this paper confirms the advantage of supercapacitors over batteries, whose lifetime is limited to a few thousands of cycles.

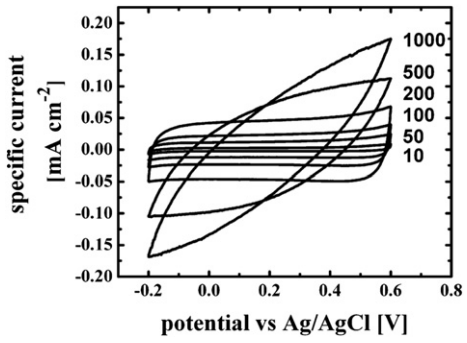


**Fig. 4.** Results of cyclic voltammetry at various scan rates (labeled in mV s$^{-1}$) for SiCNW electrode.

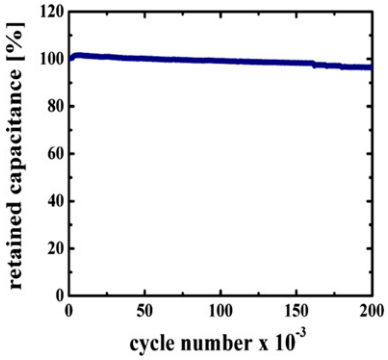


**Fig. 5.** Lifetime testing of the SiC nanowires. The charge/discharge cycles have been performed at a scan rate of 5 V s$^{-1}$.

## 4. Conclusions

We have studied the effectiveness of SiC nanowires as aqueous supercapacitor electrodes. The nanowires exhibit specific capacitance values that compare well to the state-of-the-art carbon based electrode values. Furthermore, we have demonstrated a 2 × 10$^5$ cycle lifetime without significant capacitance loss, confirming the extreme robustness of these nanowires as electrode material for supercapacitors. The current materials' capacitive behavior begins to degrade as the rate of charge/discharge exceeds 200 mV s$^{-1}$ due to internal resistances. Efforts to mitigate this by reducing the contact resistance between the nanowires and the substrate are ongoing. The excellent stability of SiC in harsh environments is attractive for high-temperature energy storage applications. These, however, require solid electrolytes with new coating methods for nanowires and are currently under investigation.

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